Amendments To The Claims

Please cancel Claims 1, 14, 19-20 and 26-27 without prejudice. The following list of the claims replaces all prior versions and lists of the claims in this application.

1. (Canceled).

2. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein the interconnect layer is formed over the gate structure to a thickness that is less than a height of the gate structure.

3. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein the mask layer is formed by an anneal process.

4. (Currently amended) The method of ~~Claim 1~~ Claim 15, further comprising removing the mask layer after removing the planarized cap layer.

5. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein a first removal rate of the interconnect layer during the planarizing is greater than a second removal rate of the cap layer during the planarizing.

6. (Original) The method of Claim 5 wherein the first removal rate is at least three times greater than the second removal rate.

7. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein the cap layer is formed directly on the interconnect layer.

8. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein a portion of the cap layer is separated from the substrate by a distance that is less than the height of the gate structure.

9. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein the cap layer comprises SiO_2.

10. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein the cap layer comprises Si_3N_4.

11. (Original) The method of Claim 10 wherein the mask layer comprises SiO_2.

12. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein the removing material includes removing the cap layer and removing polysilicon.

13. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein the cap layer has a thickness ranging between 100 angstroms and 2000 angstroms before planarizing.

14. (Canceled).

15. (Currently amended) ~~The method of Claim 14~~ A method of manufacturing a semiconductor device, comprising:

forming a gate structure over a substrate;

forming an interconnect layer over the gate structure and the substrate;

forming a cap layer over the interconnect layer;

planarizing the interconnect layer and the cap layer to form a substantially planar surface, the substantially planar surface having a portion of exposed interconnect layer and a portion of exposed cap layer; and

forming a mask layer over the exposed portion of the planarized interconnect layer; and removing material underlying the exposed portion of the planarized cap layer;

wherein the planarizing includes chemical-mechanical polishing (CMP); and

wherein the CMP includes planarizing the cap layer and the interconnect layer between a rotatable polishing head and a rotatable polishing platen at a polishing head speed ranging between 75 rpm and 200 rpm.

16. (Currently amended) The method of ~~Claim 14~~ Claim 15, wherein the CMP includes ~~planarizing the cap layer and the interconnect layer between a rotatable polishing head and a rotatable~~ rotating the polishing platen at a platen speed ranging between 65 rpm and 150 rpm.

17. (Currently amended) ~~The method of Claim 14~~ A method of manufacturing a semiconductor device, comprising:

forming a gate structure over a substrate;

forming an interconnect layer over the gate structure and the substrate;

forming a cap layer over the interconnect layer;

planarizing the interconnect layer and the cap layer to form a substantially planar surface, the substantially planar surface having a portion of exposed interconnect layer and a portion of exposed cap layer; and

forming a mask layer over the exposed portion of the planarized interconnect layer; and removing material underlying the exposed portion of the planarized cap layer;

wherein the planarizing includes chemical-mechanical polishing (CMP); and

wherein the CMP includes planarizing the cap layer and the interconnect layer between a rotatable polishing head and a rotatable polishing platen at a planarizing pressure ~~ranging~~ of at least 5.0 psi.

18. (Currently amended) The method of ~~Claim 1~~ Claim 15, wherein the device is a split gate field effect transistor.

19. (Canceled).

20. (Canceled).

21. (Withdrawn - Currently amended) ~~The method of Claim 20~~ A method of planarizing topographic features on a substrate, comprising:

providing a substrate having a plurality of layers formed thereon, the layers forming a plurality of topographic features of varying heights relative to a reference plane that is parallel to a principal plane of the substrate;

coupling the substrate to a rotatable polishing head;

contacting the topographic features with a rotatable polishing platen; and

maintaining the contacting while rotating at least one of the polishing head and the polishing platen, thereby removing portions of the topographic features to form a substantially planar surface;

wherein the rotating includes rotating the polishing head at a speed ranging between 75 rpm and 200 rpm.

22. (Withdrawn - Currently amended) ~~The method of Claim 21~~ A method of planarizing topographic features on a substrate, comprising:

providing a substrate having a plurality of layers formed thereon, the layers forming a plurality of topographic features of varying heights relative to a reference plane that is parallel to a principal plane of the substrate;

coupling the substrate to a rotatable polishing head;

contacting the topographic features with a rotatable polishing platen; and

maintaining the contacting while rotating at least one of the polishing head and the polishing platen, thereby removing portions of the topographic features to form a substantially planar surface;

wherein the contacting is done at a pressure of at least 5.0 psi .

23. (Withdrawn - Currently amended) The method of ~~Claim 20~~ Claim 21, wherein the rotating includes rotating the polishing platen at a speed ranging between 65 rpm and 150 rpm.

24. (Withdrawn - Currently amended) The method of Claim 23, wherein the speed of the polishing platen is 87 rpm.

25. (Withdrawn - Currently amended) The method of ~~Claim 20~~ Claim 21, wherein the plurality of layers includes an interconnect layer formed over a semiconductor device gate structure and a cap layer formed over the interconnect layer, wherein portions of the interconnect layer are removed at a slower rate than portions of the cap layer are removed.

26. (Canceled).

27. (Canceled).